REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-7, 9-11, 14-44, 46-48, 51-74 and 78-80 are presently active. Claims 75-77 and 81 were previously cancelled. Claims 8, 12-13, 45, and 49-50 have been presently canceled. Claims 1, 23, 28, 38, 60, 65, 78, and 79-80 have been presently amended. No new matter has been added.

Status of Claims: Claims 1, 8, and 75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al (U.S. Pat. No. 6,802,045) in view of Jain et al (Mathematical-Physics Engines: Parallel Processing for Modeling and Simulation of Physical Phenomena, 1994, IEEE, pgs. 366-373) and further in view of Tan et al (U.S. Pat. No. 6,263,255). Claims 1-21, 29-30, 32-34, 37-58, 66-67, 69-71, and 74-81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Jain et al. Claims 22 and 59 stand rejected under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Jain et al and Yunemura et al (IEEE Article "Heat Analysis on Insulated Metal Substrates"). Claims 23-28 and 60-65 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al in view of Jain et al and Chen (U.S. Pat. No. 5,719,796). Claims 31, 36, 68, and 73 stand rejected under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Jain et al and Nikoonahad (U.S. Pat. No. 6,812,045). Claims 35 and 72 stand rejected under 35 U.S.C. § 103(c) as being unpatentable over Sonderman et al in view of Fatke (U.S. Pat. Appl. No. 10/472,436).

Applicants acknowledge with appreciation the consideration of this matter and the related appeals in U.S. Serial Nos. 10/673,138; 10/673,467; 10/673,501; 10/673,506; and 10/673,583 by the Board. Applicants acknowledge with appreciation the acknowledgement

by the Board that Sonderman et al does not disclose that the simulation is performed during the performance of the actual process, as recited in claim 1. See page 7 of the Board Decision dated March 5, 2010. The Board, however, agreed with the examiner that "the combination of Sonderman, Jain, and Tan discloses or suggests performing a simulation during performance of the actual process." See page 9 of the Board Decision dated March 5, 2010. The Board reasoned that:

> However, if process parameters for an actual process are being generated during the performance of the actual process, as disclosed by Tan, then it would have been obvious to one of ordinary skill in the art that the simulation would be completed earlier in time than the actual manufacturing process since the actual manufacturing process would need the parameters generated by the simulation to be executed and would therefore complete after the simulation.

Thus, the Board's decision rests on a presumption that Tan et al use actual process parameters for an actual process to complete a simulation.

Yet, this position is not supported by Tan et al. Tan et al describe at col. 2, lines 7-10, model-based real time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run. Yet, a "model-based" real time process control does not specify when the model is completed, only that the "process control" in Tan is real time.

Accordingly, to clarify Applicants' position as to their claimed invention, Claim 1 now recites:

> based on the input data for the actual process being performed by the semiconductor processing tool, setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool,
>
> solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model in a time frame shorter in time than the actual process being performed.

Support for this clarification comes from the canceled claims as well as the following sections from Applicants' specification:

> [0035] First principles physical model 106 is a model of the physical attributes of the tool and tool environment as well as the fundamental equations necessary to perform first principles simulation and provide a simulation result for facilitating a process performed by the semiconductor processing tool. Thus, the first principles physical model 106 depends to some extent on the type of semiconductor processing tool 102 analyzed as well as the process performed in the tool. For example, the physical model 106 may include a spatially resolved model of the physical geometry of the tool 102, which is different, for example, for a chemical vapor deposition (CVD) chamber and a diffusion furnace. Similarly, the first principles equations necessary to compute flow fields are quite different than those necessary to compute temperature fields. The physical model 106 may be a model as implemented in commercially available software, such as ANSYS, of ANSYS Inc., Southpointe, 275 Technology Drive Canonsburg, PA 15317, FLUENT, of Fluent Inc., 10 Cavendish Ct. Centerra Park, Lebanon, NH 03766, or CFD-ACE+, of CFD Research Corp., 215 Wynn Dr., Huntsville, AL 35805, to compute flow fields, electro-magnetic fields, temperature fields, chemistry, surface chemistry (i.e. etch surface chemistry or deposition surface chemistry). However, special purpose or custom models developed from first principles to resolve these and other details within the processing system may also be used.
>
> [0048] The present inventors have also discovered that the network architecture of Figure 3 provides the ability to distribute model results done at one processing tool 102 for one condition set, to other similar or identical tools operating later under the same or similar conditions, so redundant simulations are eliminated. Running simulations only for unique processing conditions at on-tool and standalone modules and re-using results from similar tools that have already known simulated solutions allows for rapid development of lookup libraries containing results that can be used for diagnostics and control over a large range of processing conditions. Further, the reuse of the known solutions as initial conditions for first principles simulation reduces the computational requirements and facilitates the production of simulated solutions in a time frame consistent with on-line control. Similarly, the network architecture of Figure 3 also provides the ability to propagate changes and refinements made to physical models and model input parameters from one simulation module to others in the network. For example, if during process runs and parallel executions of a model it is determined that some input

parameters need to be changed, then these changes can be propagated to all other simulation modules and tools via the network.

[0056] In step 405, a first principles simulation processor, such as the processor 108 of Figure 1, uses the input data of step 401 and the first principles physical model of step 403 to execute a first principles simulation and provide a virtual sensor measurement. Step 405 may be performed either at a different time, or concurrently with the process performed by the semiconductor processing tool. Simulations run not concurrently with the wafer process may use initial and boundary conditions stored from previous process runs with the same or similar process conditions. As noted with respect to Figure 2 above, this is suitable in cases when the simulation runs slower than the wafer process; time may be used between wafer cassettes and even during tool shutdowns for preventive maintenance, for example, to have the simulation module solve for required measurements. These "measurements" can later be displayed during the wafer process as if they were solved for concurrently with the wafer process, and if the process is executed under the same process conditions as the simulation was run.

[0071] The simulation module 606 is a computer, workstation, or other processing device capable of executing first principles simulation techniques to control a process performed by the tool 602, and therefore may be implemented as the simulation module 302 described with respect to Figure 3. Thus, the simulation module 602 includes the first principles physical model 106 and the first principles simulation processor 108 described with respect to Figure 1, as well as any other hardware and/or software that may be helpful for executing first principles simulations to control a process. In the embodiment of Figure 6, the simulation module 606 is configured to receive tool data from one or more diagnostics on the tool 602 for processing and subsequent use during simulation model execution. The tool data may include the aforementioned fluid mechanic data, electrical data, chemical data, thermal, and mechanical data, or any of input data described with respect to Figures 1 and 2 above. In the embodiment of Figure 6, the tool data can be utilized to determine boundary conditions and initial conditions for a model to be executed on the simulation module 606. The model can, for example, include the aforementioned ANSYS, FLUENT, or CFD-ACE+ codes, to compute flow fields, electro-magnetic fields, temperature fields, chemistry, surface chemistry (i.e. etch surface chemistry or deposition surface chemistry), etc. The models developed from first principles

> can resolve details within the processing system in order to provide an input for process control of the tool.

Tan et al do not disclose or suggest solving computer-encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool in a time frame shorter in time than the actual process being performed.

Applicants' position on this matter is supported by the fact that Tan et al teach the use on an ***existing*** process model for feedback or feed forward processing. In feedback control, by definition, the results of a process step are provided to a subsequent wafer. In the feed forward control of Tan et al, the results of a prior process step are used to adjust a subsequent process being run of the wafer. Indeed, as noted below, the metrology machine 206 of Tan et al measures post-process data, and by definition could then not set initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool based on the input data for the actual process being performed by the semiconductor processing tool. Tan et al describe:

> The illustrative APC Framework 200 includes a process model 202 that receives ***feed-forward and feed-back data*** and calculates a processing parameter. The illustrative portion of the APC Framework 200 includes two measurement devices, in particular a pre-process metrology machine 204 and a post-processing metrology machine 206. The pre-process metrology machine 204 performs a measurement on a material prior to processing in a processing machine 208 and sends the measurement, as feed-forward data, to the process model 202. The processing machine 208 sends processed material to the post-processing metrology machine 206 ***to measure post-process data which is sent to the process model 202 as feedback data***.
>
> Referring to FIG. 4, a schematic block diagram shows material flow of a processing step 400 of a semiconductor manufacturing process from a process engineer perspective. An APC plan 402 ***retrieves a process model*** from the data store 306, then executes a parameter calculation algorithm 404. The APC plan 402 gives the calculated parameters to a machine 406 and directs the machine 406 to execute the process. The machine 406 issues a signal to the APC plan 402 ***when the process execution is complete***. The APC plan 402 sends the calculated parameters to the data history store 310 of the historical database 312.

> Referring to FIG. 5, a schematic block diagram shows material flow of a post-process measurement step 500 of a semiconductor manufacturing process from a process engineer perspective. An APC plan 502 sends a message to a machine 504 instructing the machine 504 to measure a post-processed material. The machine 504 sends measurement data to the APC plan 502. The APC plan 502 retrieves an old process model from the data store 306. The APC plan 502 executes a model update algorithm 506. The APC plan 502 ***stores an updated model in the data store 306 for usage in the processing step 400***. The APC plan 502 sends new model data to the data history store 310 of the historical database 312. [Emphasis added.]

Thus, Tan et al use post-process data to ***update and store*** a model fo***r a subsequent processing step***. It is the updated model (based on data measured from a prior run) that is used to control the next process run, thereby providing model-based real time process control during the process run where the model is based on data from a previous run producing an updated and stored simulation result for process control.

In other words, in Tan et al, the solution to model exists from previous runs, and essentially the whole detailed description of Tan et al revolves around the issue of how one can keep these models up-to-date as wafers are processed. Figure 2 of Tan et al (reproduced below) shows explicitly the use of "feed-forward data" and "feed-back data" for process control modifications. Figure 3 of Tan et al shows explicitly the use of "pre-process metrology" in what would be a feed-forward control scheme. Figures 4 and 5 describe the use of an updated model to control a subsequent process.

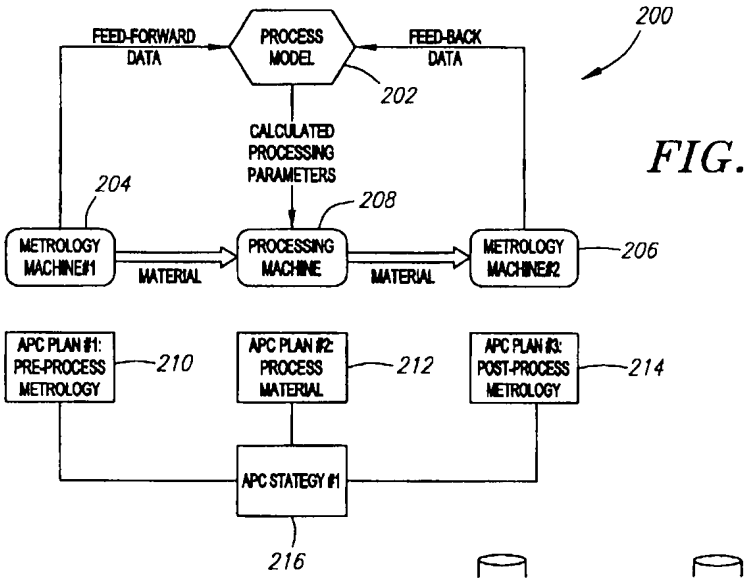


FIG. 2

Figures 6-24 of Tan et al merely provide implementation details as to the processing described above.

In short, Applicants submit that they were the first to technically realize a way to solve computer-encoded differential equations of a first principles simulation model for a spatially resolved model of a semiconductor processing tool in a time frame shorter in time than the actual process being performed in the semiconductor processing tool.

The attached declaration by Andrej Mitrovic, one of the named inventors, attests to the fact that neither Sonderman et al nor Tan et al use a first principles simulation model. Rather, the models in these references are 1) simplified models based on former approximate solutions or 2) statistical or "learned" models tracking how the systems are expected to behave.

With respect to Jain et al, Jain et al describe at pages 372-373 that:

> We ***propose*** a wafer scale implementation of the MPE. The starting point would be a dedicated processing cell, optimized specifically for the PDE arithmetic and data routing. Because of the relative simplicity of the cell, it is expected that extremely large arrays (8x8 to 32x32) ***could be*** successfully processed on a single piece of silicon using Wafer Scale Integration techniques. In fact, we have already laid the foundation for the development

> of such a processing cell. Our Universal Multiply-Subtract-Add [11] ***could be*** adapted for this first cell design. Similarly, our nonlinear coprocessor cell [12]-[14] ***might be used*** in conjunction with the UMSA to provide advanced mathematical functions. As suggested in Fig. 2, there would be ***courtyards of processors***, each with two interconnection networks and two memory banks. 2-D, 3-D, and 4-D problems could then be mapped for parallel computations. Since inter-processor delays are very small (say a few ns), extremely high speeds could be achieved. This, together with the high degree of parallelism, would result also in high throughout. We ***envision*** 100 to 1000 processors (on one wafer) forming a wafer scale MPE. At a clock frequency of 50 MHz, a single wafer could achieve up to 20 GFLOPs performance. With our nonlinear coprocessor added, each instruction could equate to multiple floating point operations.
>
> Furthermore, because of the extendible architecture, several wafers ***could be*** interconnected as shown in Fig. 5 to construct a "stacked" MPE wafer system (SMPE). Note that no vertical interconnects within the stack of wafers are expected. Tens to hundreds of GFLOPs performance in a volume the size of a desk-top computer [15] ***could*** thus be achieved. However, ***these predictions*** ignore the likely technical advances in the next five years; a tenfold further increase in performance ***might be achievable***. [Emphasis Added]

Thus, as emphasized above, the proposed development work in Jain et al requires the development of ***futuristic*** computational equipment which one of ordinary skill in the art would be reluctant to implement or utilize for the rigorous standards needed in semiconductor manufacturing. Yet, the prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986) The Court in *In re Gangadharam*, 889 F.2d 1101, 13 U.S.P.Q.2d 1568 (Fed. Cir. 1989) explained that:

> References must be considered for all that they teach. W.L. Gore & Assoc. v. Garlock, Inc., 721 F.2d 1540, 1550, 220 USPQ 303, 311 (Fed.Cir.1983), cert. denied, 469 U.S. 851 (1984). . . . A reasonable reading of the article by one of ordinary skill in the art could be that such an individual would not be informed one way or the other regarding the success of CQQ in mammals. Indeed, Schnitzer, Hawking, Experimental Chemotherapy, Vol. II Chemotherapy of Bacterial Infections Part I, (1964), indicates that perhaps one of ordinary skill in the art would not conclude, based on the results of the tests in the Gangadharam article, that there would be a reasonable expectation of success using CQQ in mammals.

Here, as attested to in the attached declaration, with the computing capability of Jain et al representing futuristic, unrealized capability, there is no reasonable expectation of success that computer-encoded differential equations of a first principles simulation model for a spatially resolved model of a semiconductor processing tool could have been solved in a time frame shorter in time than the actual process being performed in the semiconductor processing tool.

Support for Applicants position is found in the following three references

1) U.S. Pat. No. 6,185,472;
2) U.S. Pat. No. 7,047,095; and
3) U.S. Pat. No. 6,587,744.

The first reference describes a simulator that can be used "proceding semiconductor manufacturing processes" or for "correcting" predetermined schedules "without using testpieces." See col. 5, line 11-21. In other words, the simulator simulates process conditions and predicts outcomes based on the simulation such that optimized process recipes can then be used. In this aspect, U.S. Pat. No. 6,185,472 is similar to Tan et al.

The improvements in ab intio calculations described in U.S. Pat. No. 6,185,472 merely allow a "prediction" new process pathways by which semiconductor materials can be processed. Column 74 of U.S. Pat. No. 6,185,472 shows a reduction in processing time from 15900 minutes to 159 minutes for the ab initio simulations. This timeframe for one simulation would still be too long and unworkable for real time process simulation and control.

The second and third references merely describe feedback and feedforward process control where the result of a simulation would not be obtained during the performance of the actual process to control the actual process being performed, and therefore would not be used to control the actual process performed by the semiconductor processing tool. In this aspect, U.S. Pat. No. 7,047,095 and U.S. Pat. No. 6,587,744 are similar to Tan et al.

The second reference describes in the Summary Section:

> In the system achieved in the first aspect or in the method achieved in the second aspect, the control device may engage the transfer apparatus to transfer the workpieces at least having undergone the processing executed by the processing apparatus to the measuring apparatus, compare a measurement value indicating the results of the processing having been executed on a workpiece which is obtained through the measuring operation executed by the measuring apparatus on the workpieces at least having undergone the processing, with a target value for the processing results, and reset the processing conditions for the processing apparatus in correspondence to an error in the measurement value relative to the target value if the error is judged to be equal to or greater than a specific value. It is to be noted that the measuring operation may be executed on the workpiece before and after undergoing the processing, instead of executing the measuring operation only on the workpiece having undergone the processing.
>
> The workpiece at least having undergone the processing executed by the processing apparatus may be transferred by the transfer apparatus to the measuring apparatus which then executes a measuring operation on the workpiece at least having undergone the processing. The control device may compare a measurement value indicating the results of the processing having been executed on the workpiece obtained based upon the results of the measuring operation by the measuring apparatus with a target value for the processing results, observe the state of the fluctuation of an error in the measurement value relative to the target value so as to predict the tendency of the fluctuation and adjust the processing conditions for the processing apparatus in correspondence to the tendency of the fluctuation error before the error exceeds a predetermined value. It is to be noted that in this case, too, the measuring operation may be executed on the workpiece before and after the processing instead of executing the measuring operation only on the workpiece having undergone the processing.

The third reference describes in the Abstract:

> A[n] automated run-to-run controller for controlling manufacturing processes comprises set of processing tools, a set of metrology tools for taking metrology measurements from the processing tools, and a supervising station for managing and controlling the processing tools. The supervising station comprises an interface for receiving metrology data from the metrology tools and a number of variable parameter tables, one for each of the processing tools, collectively associated with a manufacturing process recipe. The supervising station also includes one or more internal models which relate received metrology data to one or more variables for a processing tool, and which can modify variables stored in the variable parameter table to control the process tools using feedback and/or feed-forward control algorithms. Feed-forward control algorithms may, in certain embodiments, be used to

> adjust process targets for closed loop feedback control. The supervising station may have a user interface by which different feedback or feed-forward model formats (single or multi-variate) may be interactively selected based upon experimental or predicted behavior of the system, and may also permit users to utilize their own models for run-to-run control.

Finally, in support of Applicants' position on this matter, the attached declaration attests to the fact that, prior to the filing of this application, a two-dimensional axisymmetric time-evolution temperature simulation of a chuck with a wafer, a plasma heat load, and a coolant heat removal was performed by myself. By setting initial and boundary conditions to values appropriate for the physical chuck setup, a time-evolving solution was obtained in less than 5 seconds, for a process of nominal duration of 60 seconds.

This simulation time gave a 12:1 factor time compression available for altering the controls to prevent running into "out-of-spec" process conditions, based on the prediction. This simulation result in less than 5 seconds occurred with all temperatures initialized to 0 deg C.

If an actual temperature at each time step from a previous wafer run had been used for initialization, the solver would not have had to make that many equilibrium iterations on each time step, even further shortening the time of solution.

As explained in the declaration, this result utilized a single core PC, with 1 GB of RAM (~2002), using ANSYS general-purpose simulation code, without any parallelization, and represented at the time an unexpected result.

For all of these reasons given above including the newly presented clarified claims and declaration evidence, Claims 1-7, 9-11, 14-44, 46-48, 51-74 and 78-80 should be found non-obvious and passed to allowance.

Regarding the rejection over Sonderman et al, Jain et al, and Chen with regard to

dependent Claims 23-28 and 60-65, the attached declaration attests to the fact that Chen also is a statistical simulator. At col. 5, line 38, to col. 6, line 25, Chen describes the use of a fitting function for fitting already simulated and measured data, not as a solution of a first principle simulation.

The full paragraph of Chen containing this citation is reproduced below with the Examiner's underscored emphasis shown:

> Corresponding steps of the simulation process 450 are performed in parallel with steps of the actual in-line process 420. A simulation start step 452 begins the simulation process 450 in response to initializing data from the actual in-line process 420. The wafer start step 422 generates initial data, such as orientation data, that is measured and transferred to the simulation process 450, typically through a manufacturing control system, such as Workstream™, the remote access channel of the manufacturing control system, such as Remote Workstream™, and a network connection to the application server, such as TCP/IP. A simulation start step 452 initializes parameters of the simulation process 450 to arbitrary, used-defined values. Following the simulation start step 452, a simulation step 454 simulates the actual process step performed in single process step 424, first using arbitrary, user-defined parameters and later adapting the parameter values on the basis of actual in-line measurements. Various miscellaneous input parameters such as processing time are designated by the test operator. These input parameters are applied to the single process step 424 and the simulation step 454. Input data may be applied in several formats. However, the input data is converted into a statistical distribution function before actual processing begins. For an array of input data points, data is sorted and the probability of a data value being between any two consecutive data points is assumed to be the same. For data presented in statistical form, such as data with a mean, standard deviation and range limits, the data is modeled in a statistical distribution function as a truncated Gaussian profile for usage as a statistical distribution function. For data presented in a statistical form, such as a mean and range limits, the data is modeled in a statistical distribution function as a truncated Gaussian profile with each specified limit being presumed to deviate from the mean value by three standard deviations. If the mean is not centered between the range limits, the function is modeled as an asymmetric profile and is considered the combination of two half-Gaussian profiles that have the same population and different standard deviations. For data presented in a statistical form, such as a mean and standard deviation, the data is modeled in a statistical distribution function as a Gaussian profile. Data presented as a single data point is used only for parameters that are insignificant when no additional information is unavailable. Each actual or simulation result, including intermediate results, is applied to the simulation and process as a statistical distribution function, rather than a single data point. Thus, a statistical distribution function is the elementary data type in the simulation system 200.

Once again, Appellant sees no disclosure in Chen of:

> calculating ***a solution*** to the first principles simulation ***by applying a close-fitting solution*** to thereby set initial conditions for cells in the first principles simulation.

Rather, the attached declaration attests to the fact that this section of Chen is directed to the arithmetic manipulation of input data, and is not directed to any kind of solution, much less a "close-fitting solution," to a first principles simulation, as defined in Claims 23-26 and 60-63.

Thus, a combination of Chen with Sonderman et al and Jain et al and Tan et al would not yield these claim features.

Furthermore, there is no disclosure in Chen for the features defined in Claims 27-28 and 64-65 regarding choosing a coarse grid for a solution of the first principles simulation (Claims 27 and 64) and then using the solution for coarse grid in a fine grid simulation (Claims 28 and 65).

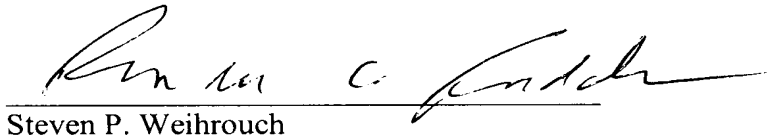
Thus, for all these reasons, a combination of Chen with Sonderman et al and Jain et al would not produce the feature in Claims 23-28 and 60-65.

Hence, for this additional reason (besides their dependence from allowable claims), the 35 U.S.C. § 103(a) rejection of Claims 23-28 and 60-65 as being unpatentable over Sonderman et al, Jain et al, and Chen should be reversed.

Conclusion: In view of the present amendment and in light of the above discussions, the application as amended herewith is believed to be in condition for appeal. An appeal brief will follow.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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